In the Specification:

Please insert after paragraph 56 the following text:

BRIEF description of the drawings

Figure 1 is a block diagram of a conventional communication system including error detection and correction.

Figure 2 is a block diagram of a communication system including error detection and correction circuitry according to one embodiment of the present invention.

Please amend paragraphs 2 and 3 as follows:

[2] In its more general aspect, embodiments of the present invention relate~~relates~~ to ~~a~~ methods and systems for applying the self-corrector code theory to digital information coded as symbol sequences, for example in the Boolean logic, stored in electronic memory systems or transmitted from and to these systems.

[3] More particularly, an embodiment of the invention relates to a method as above providing the transmission of sequences incorporating a portion of error corrector code allowing the sequence, which is more probably the original transmitted through the calculation of an error syndrome by using a parity matrix, to be restored when received.

Please amend paragraphs 4 and 5 as follows:

[4] In the specific technical field of communication systems, such as communication system 100 shown in Figure 1, it is well known that any message C comprising digital information can be processed and transferred from a system to another through electronic communication means which might be affected by noise.

[5] In substance, a sequence x of Boolean symbols transmitted by a transmitter 102 through a communication channel 104 undergoing noise can be received at a receiver 106 as a different sequence y from which it is necessary to go back to the

initial sequence x.

Please delete paragraphs 55 and 56.

Please amend paragraphs 57 and 58 as follows:

[57] Figure 2 is a block diagram of a communication system 200 including error detection and correction circuitry 201 for executing a~~A~~ method according to an embodiment of the invention. ~~is now described in detail, which~~ This method applies ~~the~~ self-corrector code theory to digital information coded as symbol sequences. The system 200 further includes a transmitter/receiver 202 that operate in conjunction with the circuitry 201 to transmit messages X and receive messages Y over and a communications channel 204.

[58] More particularly, a method according to one embodiment of the invention allows error corrections to be performed on digital information coded as symbol sequences x, for example digital information stored in electronic memory systems or transmitted from and to these systems and providing the transmission of sequences x incorporating an error corrector code portion allowing the sequence x, which is more probably the original transmitted through the calculation of an error syndrome using a parity matrix, to be restored when received. Figure 2 functionally illustrates such a memory system 206 including a memory 208 and the transmitter/receiver 202.

Please amend paragraph 89 as follows:

[89] Therefore the type of error occurred is distinguished by comparing the syndrome with the values actually received. The manufacture of a circuit describing this method involves the creation of non-binary adders as shown in Figure 2, even if they operate with a frequency of 0 and 1 (writing each number with the binary representation). If for example operation is made on Z5, the adder must be able to say that (100) + (100) = (010), i.e. 1 * 1 = 2, but (110) + (010) = (000), i.e. 3 * 2 = 5. Moreover it must be possible to find the complement of a number which will be searched in the matrix.